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# ML based PPA Push using DRV Prediction

Jungho Kim, Kyoungsun Cho, Sunghoon Kim, Mintae Lee, Wook Kim, Ki-ok Kim,  
Sangyun Kim

Samsung Semiconductor

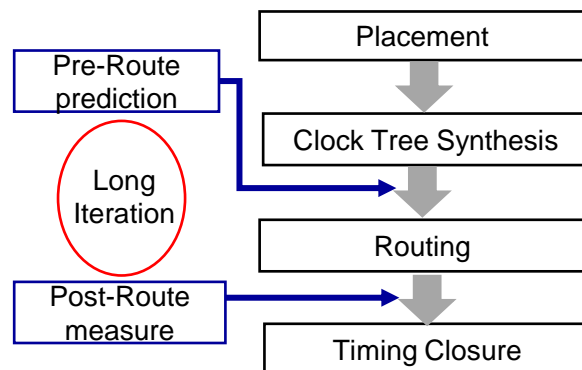


# 01 | Motivation: Increased Design Time in Advanced Processes

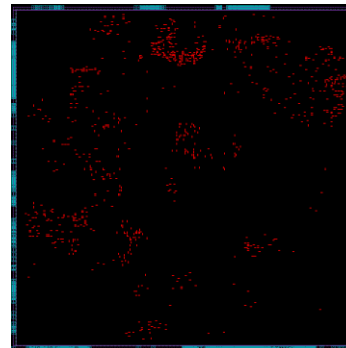
**As process technologies keep on advancing, longer physical design time with more iteration is required**

- Longer physical design time with more iteration makes hard to push PPA to limit
- DRV(Design Rule Violation) is not known until before detail routing, which is most time-consuming process, and it is hard to fix it after detail routing by routing alone and cell placement needs to be modified
- GRC(Global Routing Congestion), can no longer directly correlate the DRVs after detailed routing, what makes detailed routing necessary to verify whether DRVs occurs due to current placement in advanced process even though it is the most time consuming process
- To reduce physical design time, predict DRVs with fast runtime and moderate accuracy is required to modify cell placement before running detailed routing

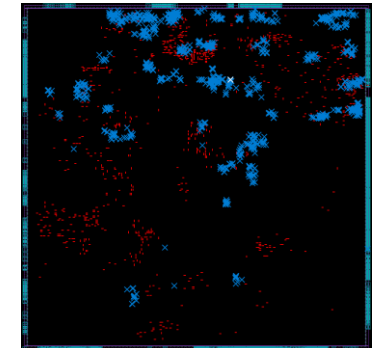
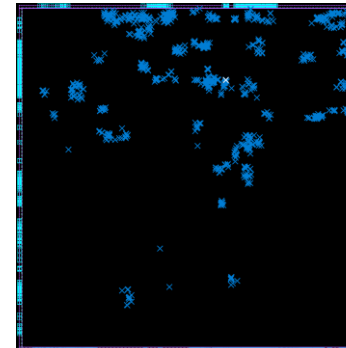
**Therefore, I would like to propose an ML based work flow that can predict the DRV after detailed routing using the global routing DB and obtain area gain using DRV aware placement method based on ML prediction**



- GRCs



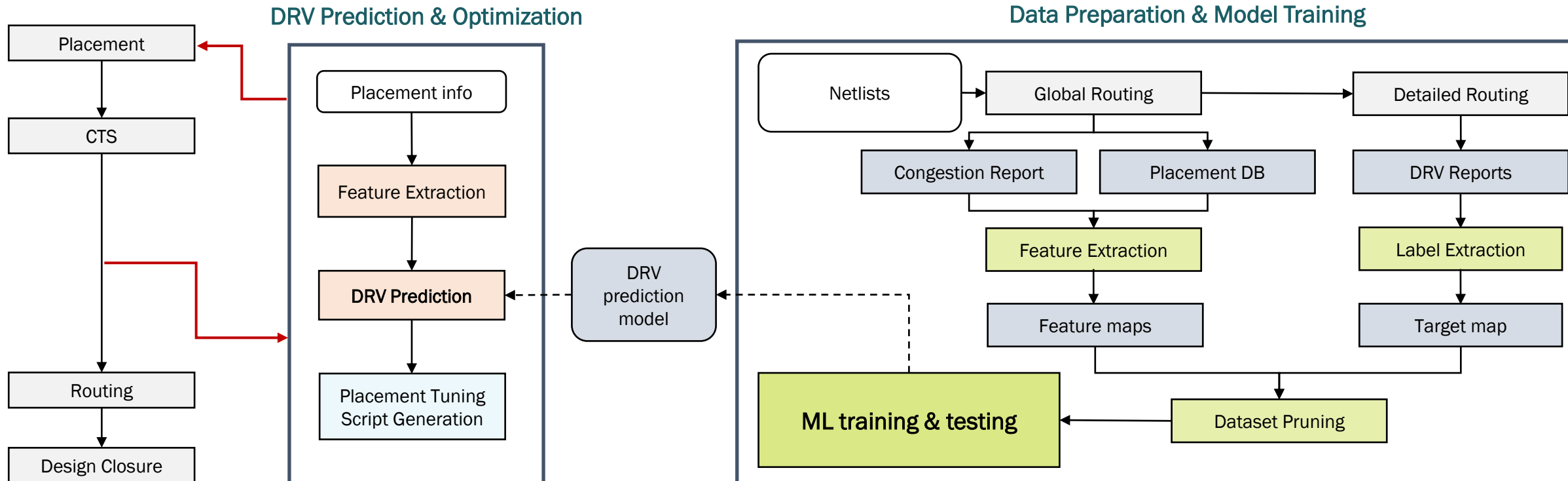
X DRVs after detail routing



# 02 | Overall of ML Based Design Flow

## ML based DRV prediction & area optimization

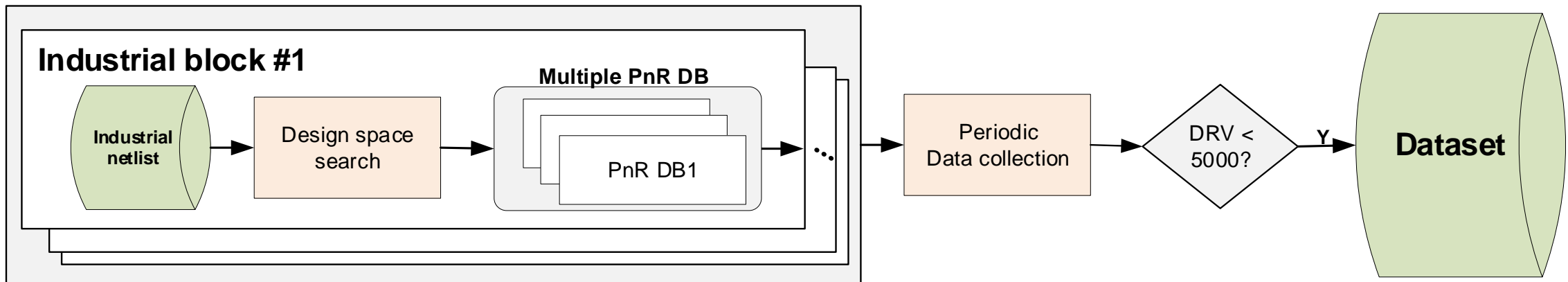
- Extract features from placement DB of pre-routed design and train the model with extracted features as inputs and DRV report from detailed routed DB as label
- Apply DRV aware placement method based on ML model to placement step
- Rerun P&R flow



# 03 | Data Collection

## Designs with macros were used to represent the trend of the industrial design

- Opencore and industrial designs at 5nm process for training dataset
- In case of Opencore, multiple placement DB were generated using reference design methodology from each netlist with various parameter settings which is still realistic.
- Industrial designs under development were collected periodically to increase the number and diversity of dataset.
- The number of DRV hotspots under 5000 were selected in order to focus on the regions of interest in DRV



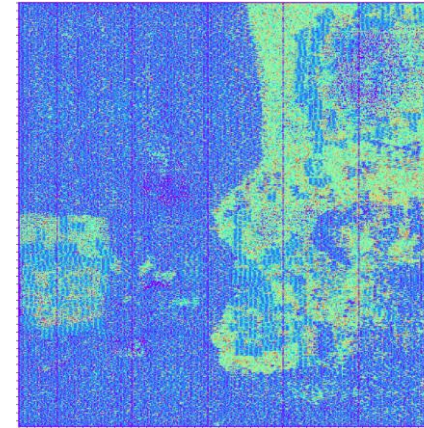
<Industrial design collection flow>



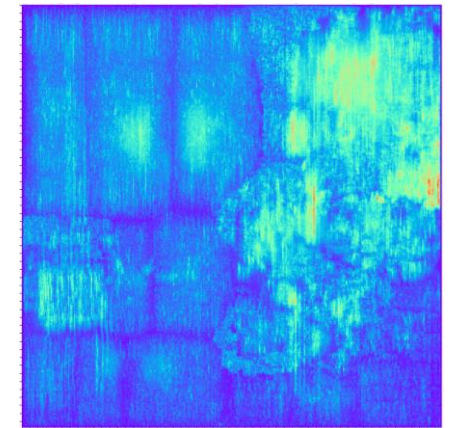
# 04 | Feature Extraction

## Grid based routing and density related features are extracted from pre-routed placement DB

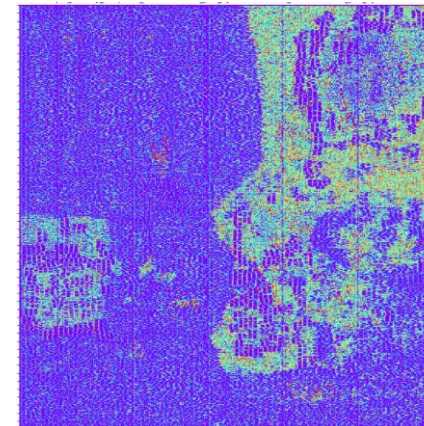
- Routing resource related features
  - Long/short<sup>[1]</sup>/pin<sup>[2]</sup> RUDY
  - H/V net density<sup>[3]</sup>: Expected number of nets passing
  - H/V congestion: Congestions
  - Global/local net: Nets connected to outside/inside grid
- Density related features
  - Pin density: Area number of pins define as M1, M2
  - Macro density: Ratio of grid occupied by macros
  - Flip-flop density: Ratio of grid occupied by flip-flops
  - Cell density: Ratio of grid occupied by cells



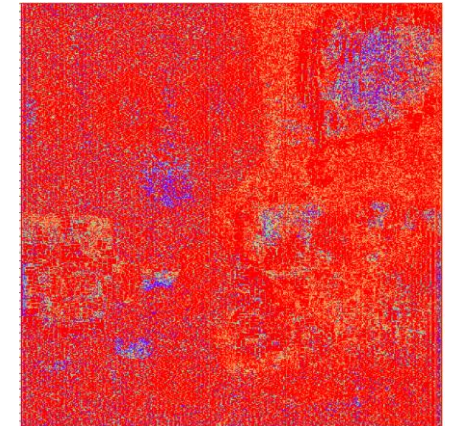
<Global net>



<Net density>



<Pin Density>



<Cell density>

[1] P. Spindler and F. M. Johannes, "Fast and accurate routing demand estimation for efficient routability-driven placement," in Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE), 2007.

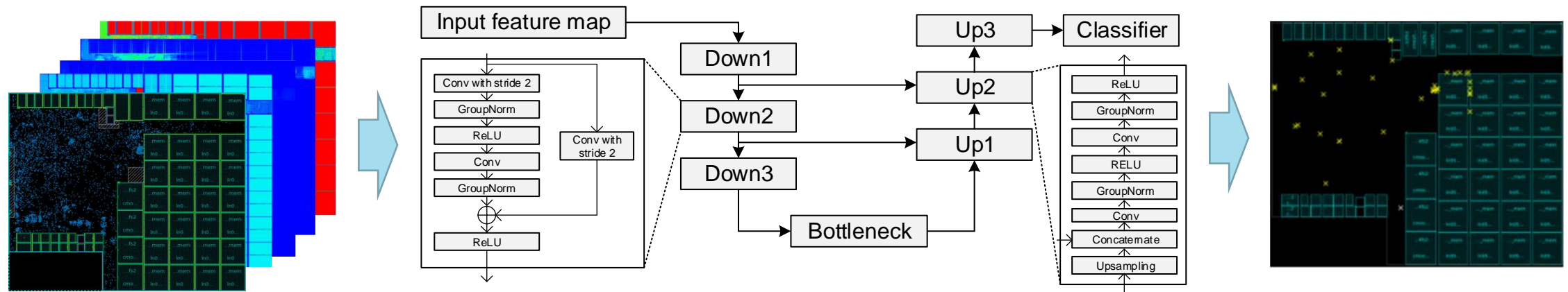
[2] Xie, Zhiyao, Yu-Hung Huang, Guan-Qi Fang, Haoxing Ren, Shao-Yun Fang, Yiran Chen, and Jiang Hu. RouteNet: Routability prediction for mixed-size designs using convolutional neural network. In 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1-8. IEEE, 2018

[3] J. Chen, J. Kuang, G. Zhao, D. J.-H. H. Huang, and E. F. Young, "Pros: A plug-in for routability optimization applied in the state-of-the-art commercial eda tool using deep learning," in Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2020.

# 05 | DRV Prediction Model

## FCN based U-net<sup>[4]</sup> network with encoder-decoder structure were used

- Network consists of a contracting path and an expansive path.
- Through contracting path, data traversing multiple convolutional network, extracting spatially abstracted information for identifying the relevant features in the input
- On the other hand, Expansive path decodes the encoded data to maintaining the spatial resolution of the input
- Blocks used contracting path are based on RESNET structure, convolution layer and short skip connections embedded.
- Expansive path combines data from contracting path through skip connection to preserve high-resolution features



[4] O. Ronneberger, P. Fischer, and T. Brox, "U-net: Convolutional networks for biomedical image segmentation," in Proceedings of International Conference on Medical image computing and computer-assisted intervention (MICCAI), 2015.

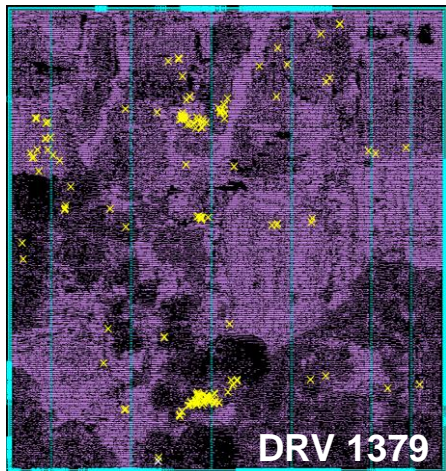


# 06 | ML Based DRV Aware Placement

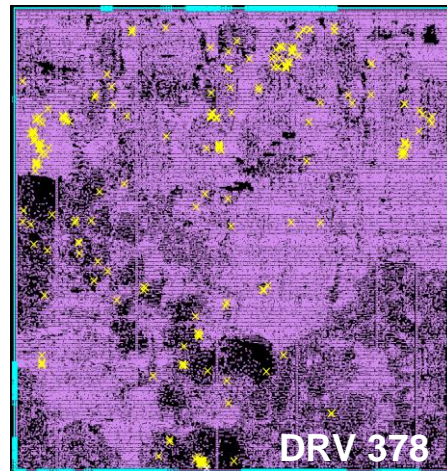
## Set keep-out margin at predicted DRV hot spot to relax cell/pin density

### → relax local routing congestion

- Excessive keep-out margin → Increases DRV violations by restricting placement of other cells  
→ Need to maintain cell padding applied to the entire cells under 10%
- If only apply keep-out margin to DRV hotspot, rearranged cells can be placed in spots that already suffer from routing resources, result in another DRV
- Prediction of the ML model shows possibilities of DRV hotspots which are spots that already ran out of routing resources even though DRV did not occur after detailed routing

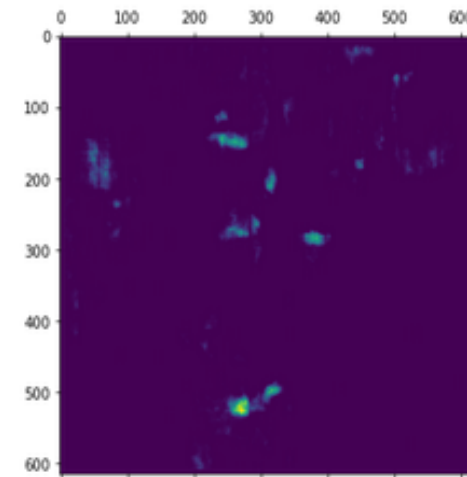


(a)

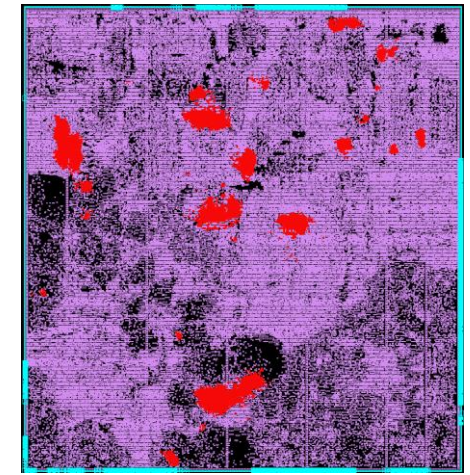


(b)

<(a)Before and (b)after applying DRV aware placement method>



(a)



(b)

<(a)Prediction of the model and (b)spots method applied>

# 07 | Experiment Results

**By using proposed ML based DRV prediction model, achieved area gain of 3% with 5nm industrial block**

- Timing, power consumption remain same after apply ML based DRV relaxation flow

**Increasing recall while not hurting F1 is effective to relax DRVs w/o side effects**

- Increasing recall is tend to include spots where DRVs are likely to occur
- Including spots with high possibility of DRV from model is effective in relex the routing congestions in spots already ran out of routing resources

**Run time < 20 min with 2.4M instances block including feature extraction**

Block	UTIL	F1 Score <sup>*</sup>	Precision <sup>**</sup>	Recall <sup>***</sup>	DRV(route)		DRV(route_opt)	
					Before	After	Before	After
Industrial Block #1	75	0.16	0.09	0.47	472	148	278	12 (96%↓)
	76.5	0.12	0.07	0.31	374	176	304	31 (90%↓)
	77	0.2	0.13	0.47	429	221	359	97 (73%↓)
	78	0.21	0.12	0.63	1379	378	877	73 (92%↓)

\*F1 score: Harmonic mean of precision and recall

\*\*Precision : Positive predictive value, accuracy of the positive predictions made by the model

\*\*\*Recall : True positive rate, measures the proportion of actual positive cases that are correctly identified by the model



## 08 | Summary

- **Proposed ML Based DRV prediction & optimization work flow that can reduce iteration and design time of physical implementation**
- **Proposed solution is also effective in solving DRVs related to density problems, and furthermore, by reducing DRVs, area gain can be obtained**
- **Controlling hyper parameter to get higher recall value while keeping F1 is effective to find spots where DRVs are likely to occur**
- **In this work, we demonstrate that P&R with the proposed placement guide can achieve 3% area gain with 92% DRV reduction**